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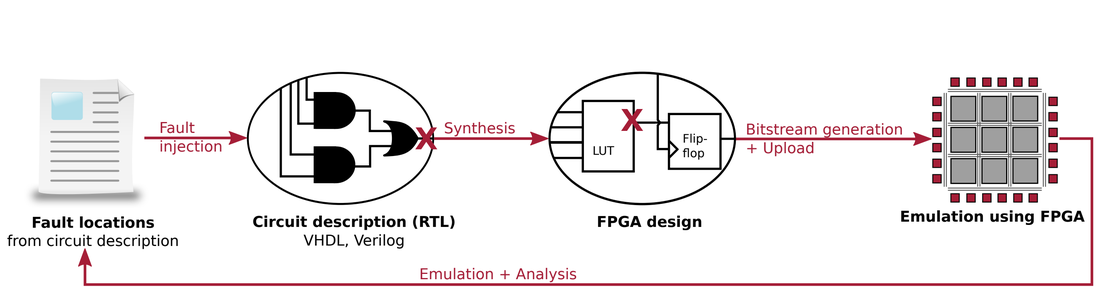
A Fast and Accurate FPGA-based Fault Injection System

Problem

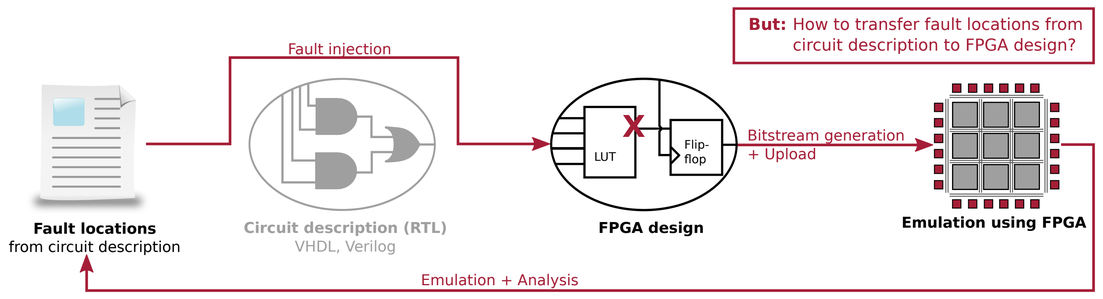
Hardware verification is too slow when using serial fault emulation.



Proposed solution

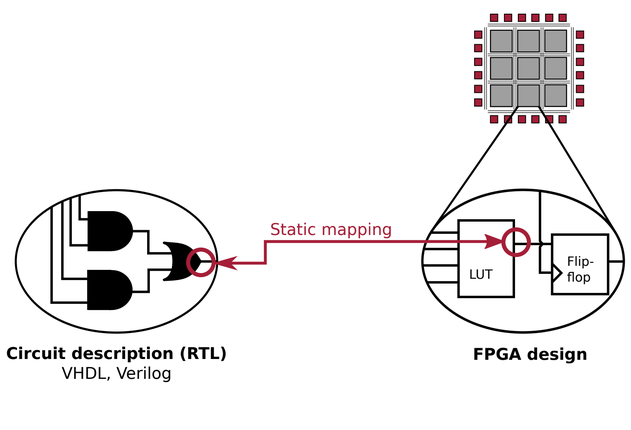
Bypassing the time-consuming synthesis by a direct injection of faults into the FPGA design.

But: How to transfer fault locations from circuit description to FPGA design?



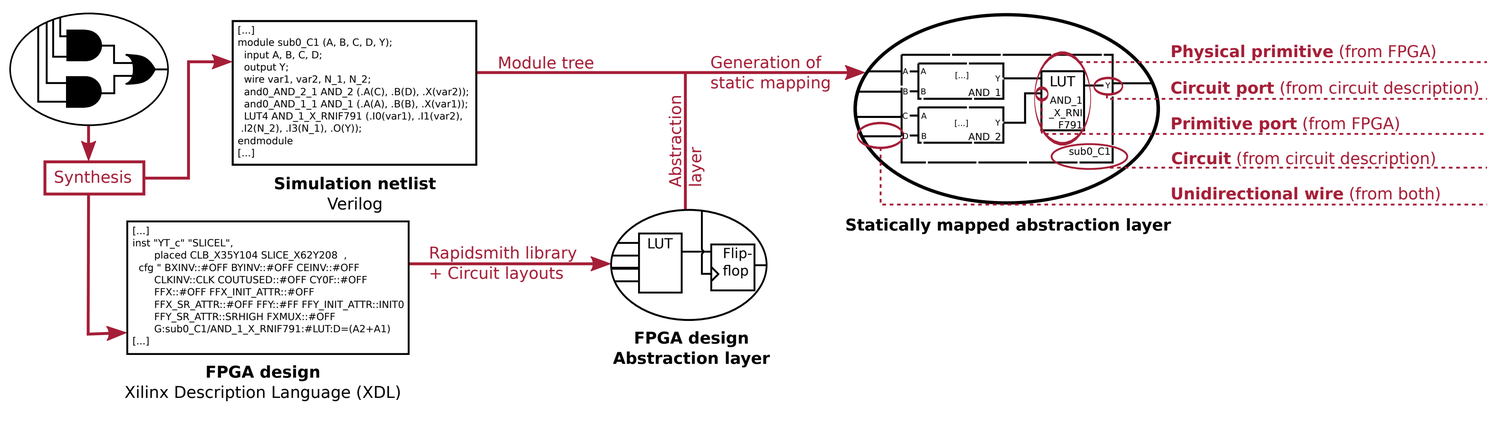
Static mapping

Need for a static mapping between FPGA design and circuit description.



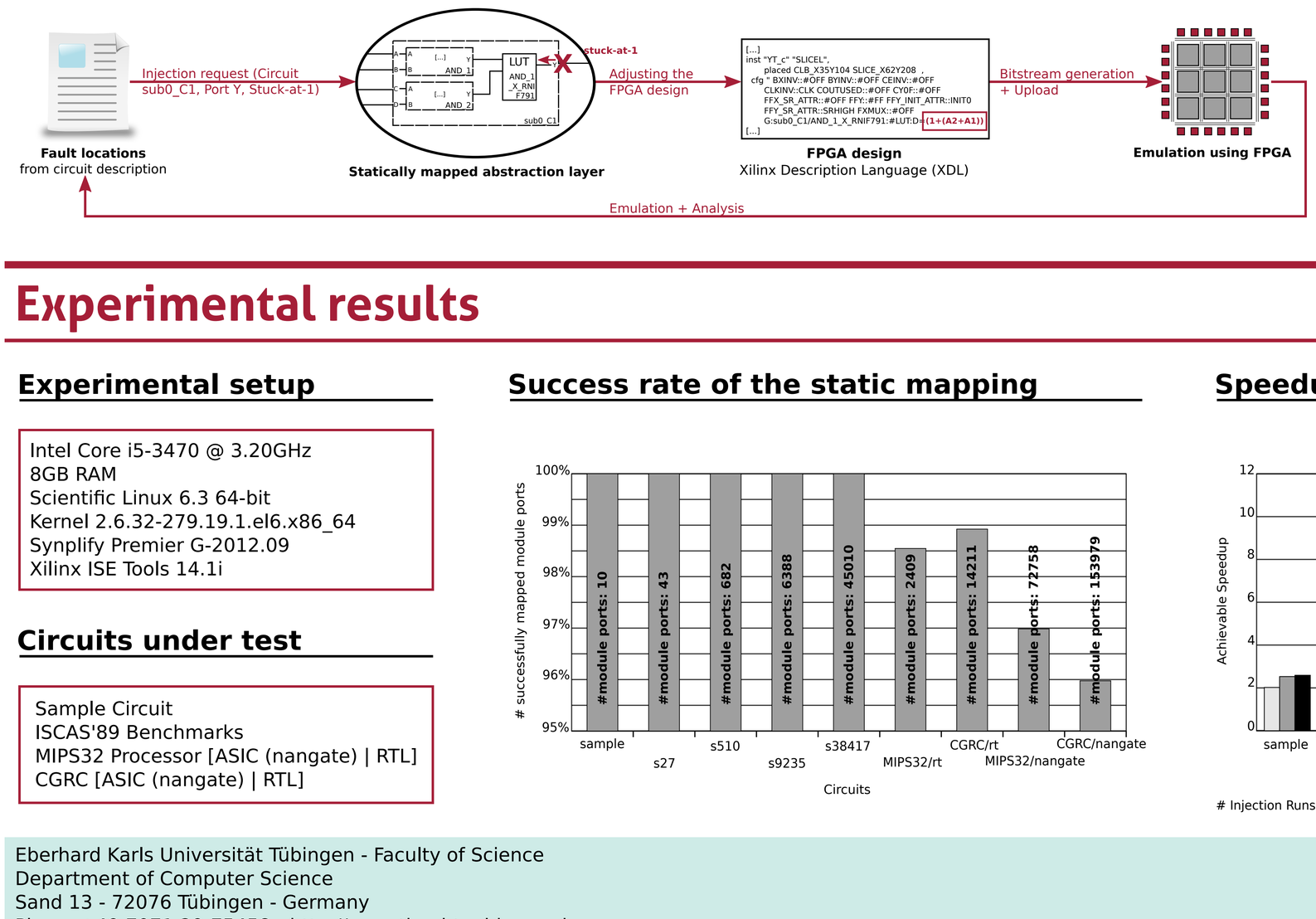
Generation of the static mapping

Creating a static mapping that provides the fault locations from the circuit description while connecting them to physical primitives on the FPGA.



Using the static mapping for the fault injection

Adjusted workflow of the serial fault emulation



Benefits & drawbacks of the proposed fault injection method

+ Faster when compared to serial fault emulation
+ More accurate when compared to JBits-based approaches.
+ Less design size when compared to instrumentation.

− Static mapping for non-port wires and registers not possible.
Solution: Move signals into separate modules and ports.

− Bitstream generation is the bottleneck of our approach.
Outlook: Bypassing bitstream generation by determining a mapping between a design and its bitstream.

Experimental results

Experimental setup

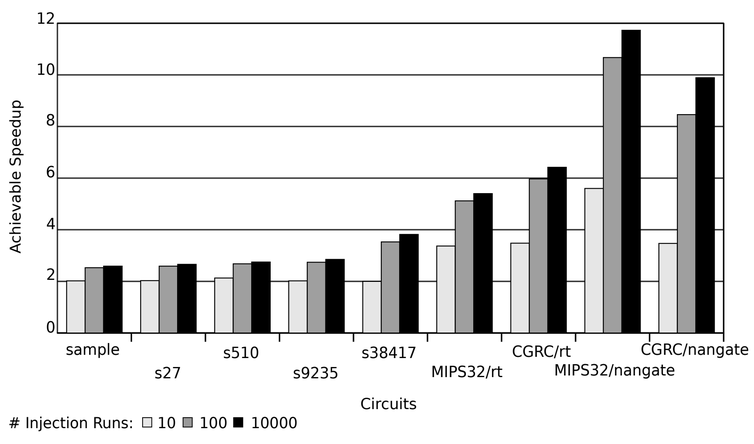
Intel Core i5-3470 @ 3.20GHz
8GB RAM
Scientific Linux 6.3 64-bit
Kernel 2.6.32-279.19.1.el6.x86_64
Synplify Premier G-2012.09
Xilinx ISE Tools 14.1i

Circuits under test

Sample Circuit
ISCAS'89 Benchmarks
MIPS32 Processor [ASIC (nangate) | RTL]
CGRC [ASIC (nangate) | RTL]

Success rate of the static mapping

Speedup compared to serial fault emulation



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